31.4 A Fully Integrated RF Front-End with Independent RX/TX Matching and +20dBm Output Power for WLAN Applications

Richard Chang[1], David Weber[1], MeeLan Lee[1], David Su[1], Katelijn Vleugels[1], Simon Wong[2]

[1]Atheros Communications, Santa Clara, CA
[2]Stanford University, Stanford, CA

The rapid growth of the wireless local area network (WLAN) market has necessitated new circuit techniques that integrate high-power power amplifiers (PAs), high-sensitivity low-noise amplifiers (LNAs), and RF transmit/receive (T/R) switch components onto a monolithic CMOS IC to alleviate the cost of external discrete components between the system-on-chip (SoC) and the antenna. The popularity of multiple-input multiple-output (MIMO) technologies has further hastened the appeal of these approaches because any external front-end components must be multiplied by the number of RF chains. While solutions exist to integrate an LNA and RF switch with a lower-power PA, the requirements to achieve +20dBm output power on a CMOS SoC often directly contradict the conditions needed for achieving a high sensitivity LNA [1-4]. This work presents an LNA and RF switch topology that can be integrated together with a +20dBm PA without compromising the LNA performance or reliability and provides independent optimal impedances for both at minimal additional silicon area.

The integrated T/R switch must be designed to support the high output power requirements of the PA, while adding minimal insertion loss for both receive and transmit paths. A +20dBm PA requires a low load impedance, high voltage supply, and large supply current. On the other hand, a CMOS LNA requires a higher optimal impedance for minimum noise figure. Inserting an integrated T/R switch using pass transistors allows the LNA and PA to share a common pathway to the antenna, but constrains them to seeing the same impedance. In this design, this incompatibility is overcome by adding a passive π impedance-transformation network in front of the LNA that also functions as the T/R switch, as shown in Fig. 31.4.1. By reusing existing pieces of the PA and LNA circuits for the π network, this RF T/R switch achieves low area usage and low-loss to minimize its impact on the noise figure.

Figure 31.4.2 shows the schematic of the LNA, which is a common-gate amplifier that provides up to 20dB of variable gain for the receiver. This topology is chosen for its flexibility in source impedance requirements, while the differential nature of the design increases the robustness of the circuit to package parasitics and common-mode noise. The input of the LNA is connected to the output of the PA by a π transformation network comprised of an inductor L_{LNA}, capacitor C_{pi}, and inductor L_{PA}. In the receive mode, the PA is shut off, and the incoming RF signal from the antenna flows through the π network into the LNA. Since the PA devices are off, it presents a minimal load to the LNA. The π network is configured to achieve the optimal noise figure impedance. The measured LNA S_{11} is better than -15dB at 2.4GHz. This LNA, when integrated with an IEEE 802.11g receiver, has an overall receive chain noise figure of 5.8dB. At 1Mb/s data rate, a -94dBm receive sensitivity is achieved. At the more demanding 54Mb/s rate, -73dBm sensitivity is achieved, as shown in Fig. 31.4.3. The LNA draws 8.4mA from a 1.8V supply.

In the transmit mode, the T/R switch ensures the reliability of the LNA by providing AC isolation from the large voltage swings and DC isolation from the high voltage supply of the PA. Series capacitance C_{pi} allows the use of thick-oxide devices and high supply voltages in the PA design without impeding the use of thin-oxide devices and low supply voltages in the LNA design. Transistor m_{SW} protects the LNA from the large transmit output signals.

To switch from receive to transmit mode, CMOS switch (m_{SW}) is turned on to short out the LNA inductor L_{LNA}. The PA inductor L_{PA} forms a parallel resonance with capacitor C_{pi} to present an open circuit to the PA, minimizing the LNA loading on the PA. Since inductance L_{PA} is a high-Q bond wire, the effectiveness of this open is only limited by the relatively high-Q capacitor C_{pi} and small on-resistance of transistor m_{SW}. This switch configuration provides over 20dB of RF isolation.

Figure 31.4.4 shows a schematic for the PA. The PA inductors L_{PA}, consisting of bondwires, are the RF chokes that supply current to the PA. The output stage is comprised of a differential cascoded common-source amplifier. To maximize the output voltage swing, a 3.5V supply is used, and a thick-oxide common-gate device is sized to protect the thin-oxide common-source device from voltages that would otherwise compromise its reliability. The gate of this cascode device is pulled to ground during RX mode to implement the required series switch to minimize loading. A thin-oxide 0.18µm core device is chosen for the common-source device due to its high transconductance, which increases the gain of the output stage and lessens the burden of the driver design. The differential topology is used to mitigate the sensitivity of the amplifier gain to the parasitic source inductance from the ground bondwires. The high linearity requirements of OFDM modulation combined with the relatively low RF gain achievable in CMOS technology lead to the choice of a class-A bias, and consequently, large DC currents are needed to achieve high RF output power. Ensuring adequate width in the metallization to avoid metal migration issues is therefore a major layout constraint, balanced by the need to keep parasitic capacitances low for 2.4GHz operation.

Figure 31.4.5 shows the measured performance of this PA when integrated with an 802.11g transmitter. The saturated output power (P_{sat}) is +25dBm. At the 6Mb/s rate, +20dBm output power can be delivered to the antenna while staying within the IEEE spectral mask requirements. At the 54Mb/s rate, the EVM requirement of -25dB can be achieved while delivering +16dBm to the antenna. The relationship of EVM to output power is shown in Fig. 31.4.6, which demonstrates that PA nonlinearity is the dominant source of modulation error in this system at higher output powers. For these measurements, the quiescent bias for the power amplifier is 300mA from a 3.5V supply. The degradation of output power due to the loading of the integrated LNA and switch is measured to be less than 1dB.

Integrating this architecture within an SoC allows all requirements of the 802.11g standard to be achieved without any active components between the SoC and the antenna. A die micrograph of this RF front-end as part of such an SoC is presented in Fig. 31.4.7. The area of the RF circuits is less than 1.2mm^2 and is implemented in a standard 0.18µm CMOS technology.

References

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[4]F.-J. Huang and K. O, "A 0.5µm CMOS T/R Switch for 900MHz Wireless Applications," *IEEE J. Solid-State Circuits*, vol. 36, pp. 486-492, March, 2001.

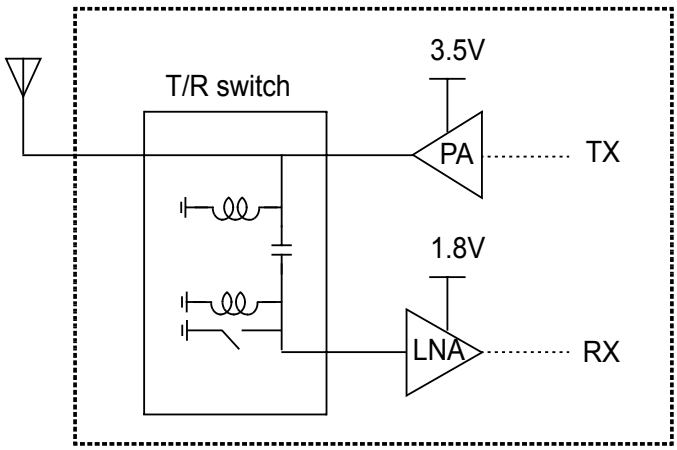

Figure 31.4.1: Block diagram of the integrated front-end.

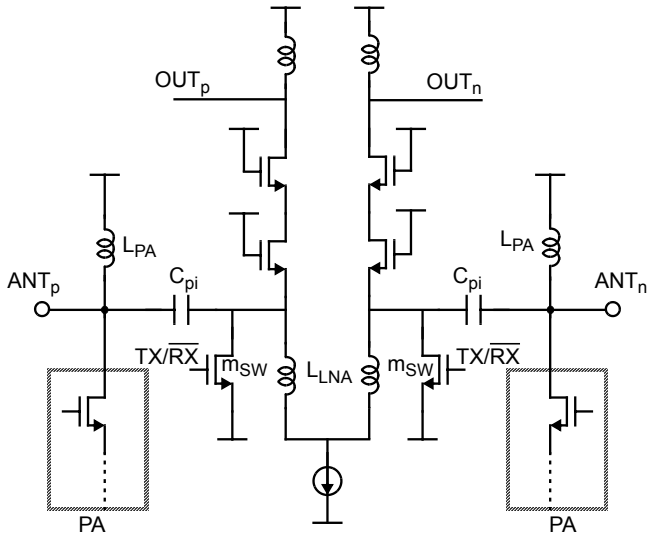

Figure 31.4.2: Schematic of the LNA and the integrated T/R switch.

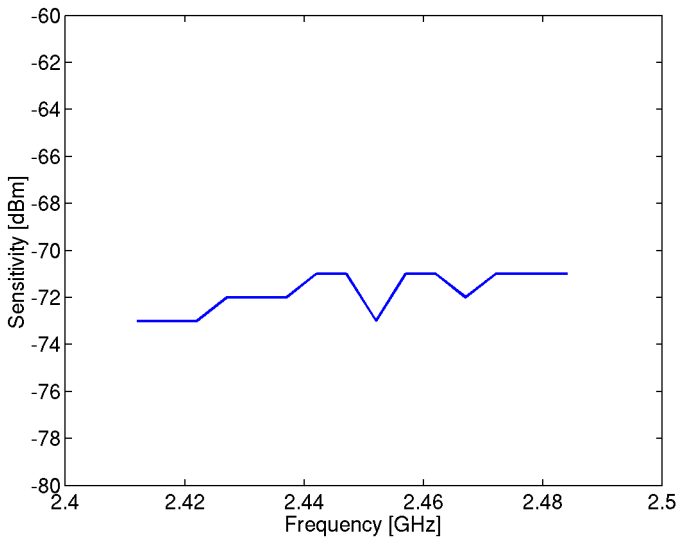

Figure 31.4.3: Receive sensitivity versus channel for a 54Mb/s rate signal.

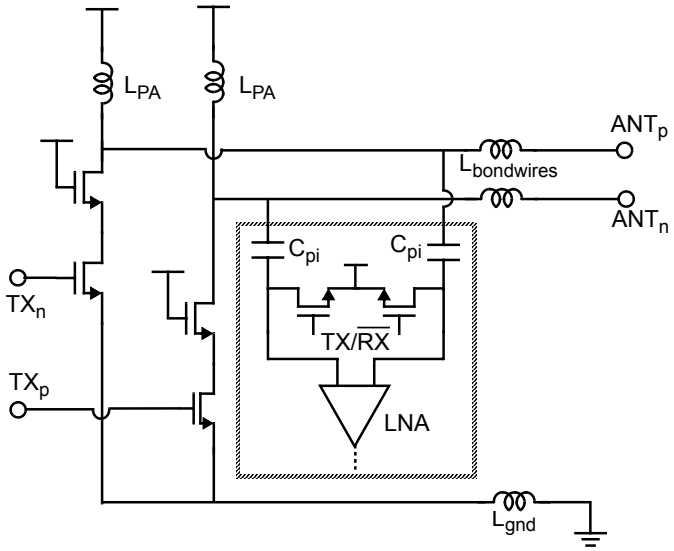

Figure 31.4.4: Schematic of the PA.

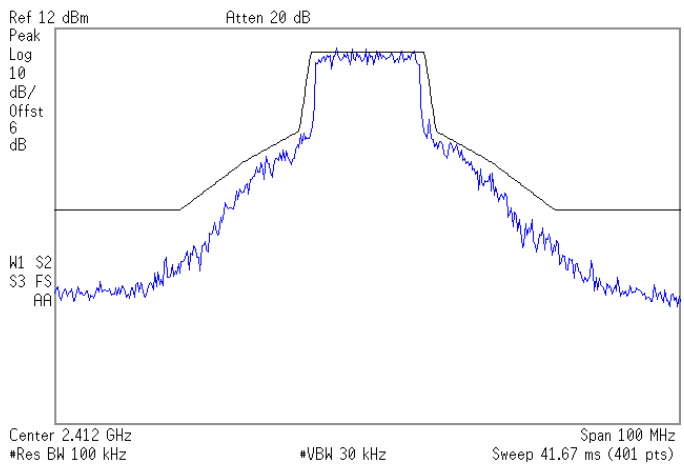

Figure 31.4.5: PA spectrum at +20dBm versus 802.11g spectral mask.

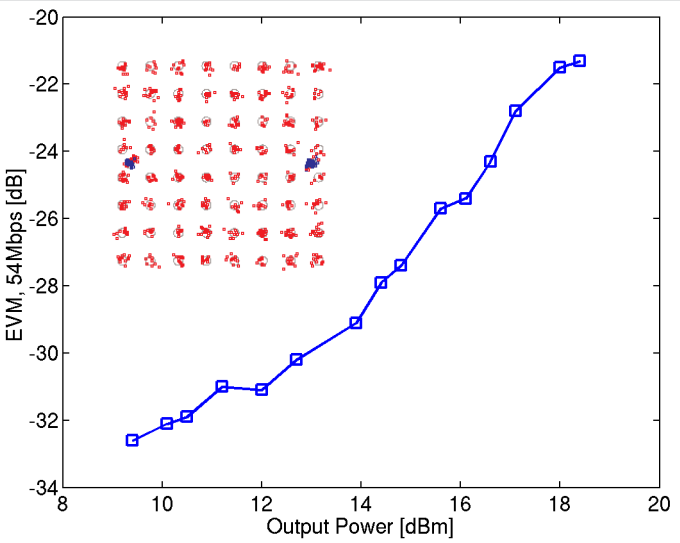

Figure 31.4.6: EVM versus TX output power with 64QAM Constellation at +16dBm output power (inset).

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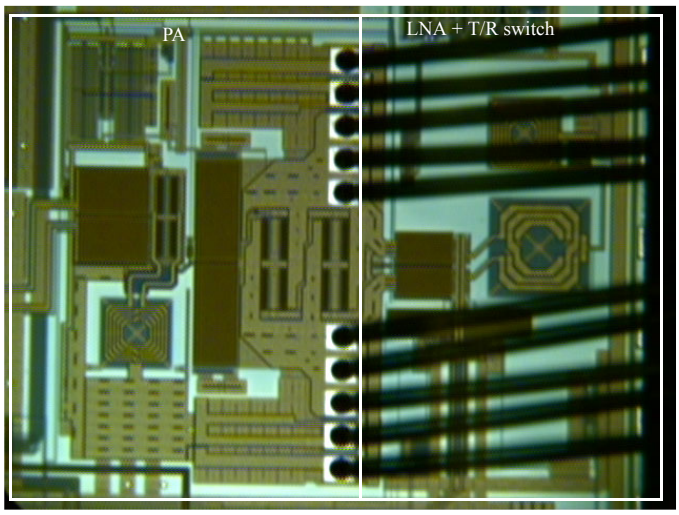

Figure 31.4.7: Die micrograph of the integrated RF front-end.

